B5 if the dummy region has the width equal to the width of the n^+ region 15 as illustrated with the solid line, or a wider width as illustrated with the broken line, the requirement is satisfied.

Please replace the paragraph on page 9, lines 5-14, with the following rewritten paragraph:

B6 After that, 5 nm thick SiO_2 is formed on the Si substrate by thermal oxidation of 800EC, and an ion implantation pattern is formed by photo lithography. There follows ion implantation of arsenic to n^+ regions under the acceleration voltage of 35 KeV by the dose of $2x10^{14}cm^{-2}$, and ion implantation of BF_2 to p^+ regions under the acceleration voltage of 10 KeV by the dose of $2x10^{14}cm^{-2}$. Subsequently, by annealing at 1000EC for 30 seconds in N_2 atmosphere, a shallow n^+ layer 113 is formed in the p-well 108 and a shallow p^+ layer 114 is formed in the n-well (Fig. 8G).

IN THE CLAIMS:

Please cancel claims 1-7 and 9-15 without prejudice or disclaimer, amend claim 8, and insert new claims 16-18 as follows:

B7 8. (Amended) The semiconductor device according to claim 16, wherein said device regions act as static RAM cells.

B8 16. (New) A semiconductor device comprising:

first and second wells opposite in conductivity types and disposed adjacent to each other;

a well isolation structure comprising a shallow trench formed on a boundary of said first and second wells;

Sub C1 a first device region provided in said first well;

a second device region provided in said second well, said first and second device regions being disposed to oppose each other, with said well isolation structure disposed between said first and second device regions;

a third device region provided in said first well;

a fourth device region provided in said second well, said third and fourth device regions being disposed not to oppose each other, with said well isolation structure disposed between said third and fourth device regions;

wherein a first width of said well isolation structure between said first and second device regions is smaller than a second width of said well isolation structure between said third and fourth device regions.

17. (New) The semiconductor device according to claim 16, wherein said first, second, third and fourth device regions have substantially same configuration.

18. (New) A semiconductor device comprising:

a first well of p type and a second well of n type disposed adjacent to each other;

a well isolation structure comprising a shallow trench formed on a boundary of said first and second wells;

a pair of a first device region of n type and a second device region of p type, said first and second device regions being disposed to oppose each other, with said well isolation structure disposed between said first device region and said second device region;

a third device region of n type and fourth device region of p type, said third and fourth device regions being disposed not to oppose each other, with said well isolation structure disposed between said third device region and said fourth device region;

wherein said first and third device regions are provided in said first well and said third and fourth device regions are provided in said second well, and a first width of said well isolation structure between said first and second device regions is smaller than a second width of said well isolation structure between said third and fourth device regions.